IN THE CLAIMS

What is claimed is:

1. A memory device, comprising:

at least a first memory cell array coupled to a read data bus that outputs read data and coupled to a separate write data bus that inputs write data, the at least first memory cell array accessing read data in response to a first type edge of a first clock and latching write data on at least the first type edge of the first clock; and

at least a second memory cell array coupled to the read data bus and coupled to the write data bus, the at least second memory cell array accessing read data in response to a first type edge of a second clock and latching write data on at least the first type edge of the second clock, the second clock being phase shifted with respect to the first clock by less than 180°.

2. The memory device of claim 1, wherein:

the first and second memory cell arrays comprise sections of n x m memory cells, and the write data bus includes m input data lines.

3. The memory device of claim 1, wherein:

the first and second memory cell arrays comprise static random access memory (SRAM) cells.

4. The memory device of claim 1, wherein:

the second clock is synchronous with, and phase shifted by about 90° with respect to the first clock.

5. The memory device of claim 1, wherein:

the first memory cell array latches write data on both the first and second type edges of the first clock; and

the second memory cell array latches write data on both the first and second type edges of the second clock.

6. The memory device of claim 1, further including:

an address bus different than the read data bus and write data bus;

a first address latch coupled between the address bus and the first memory cell array that latches an address value on the address bus in response to the first type edge of the first clock, and outputs an internal address; and

a second address latch coupled between the first address latch and the second memory cell array that latches the internal address value in response to the first type edge of second clock.

7. The memory device of claim 1, further including:

a multiplexer having one input coupled to the first memory cell array

and another input coupled to the second memory cell array that outputs read data at least four times the rate of the first clock signal.

8. The memory device of claim 1, further including:

an address bus different than the read data bus and write data bus;

a first write address decoder coupled to the first memory cell array;

a first write address register coupled to the address bus having an output coupled to a first write address decoder;

a second write address decoder coupled to the second memory cell array; and

a second write address register coupled to the first write address register having an output coupled to a second write address decoder.

9. A memory device, comprising:

a number of *N* memory cell arrays, each comprising at least two sections, the number *N* being an integer greater than 1;

a first write register that latches write data for a first of section of a first memory cell array on a rising edge of a first clock signal and latches write data for a second section of the first memory cell array on a falling edge of the first clock signal; and

a second write register that latches write data for a first section of a second memory cell array on a rising edge of a second clock signal and latches write data for a second section of the second memory cell array on

a falling edge of the second clock signal, the second clock signal have essentially the same frequency as the first clock signal but being phase shifted with respect to the first clock signal by about 180°/*N*.

10. The memory device of claim 9, wherein:

the number *N* is no less than 2.

11. The memory device of claim 9, wherein:

each memory cell array comprises *M* sections; and

the first memory cell array and second memory cell array provide a burst of *M* read data values in response to one read address.

12. The memory device of claim 11, further including:

a read output register circuit that receives *M* read data values from each memory cell array, and outputs such data as *N* * *M* words at a different phase with respect to one another.

13. The memory device of claim 9, further including:

an address latch corresponding to each memory cell array, each address latch being arranged in series in a predetermined order and latching an address value according to a phase delay with respect to a previous address latch in the series, the phase delay being about 180°/*N*.

14. The memory device of claim 9, further including:

a multiplexer for outputting read data from the memory cell arrays at a frequency of *N* * F, where F is the frequency of the first and second clock signals.

15. A method of increasing data throughput in a memory device, the method comprising the steps of:

accessing a first of *N* memory cell arrays on a first-type edge and second-type edge of a first clock signal in response to one address value;

accessing a second of the *N* memory cell arrays on a first-type edge and second-type edge of a second clock signal in response to the same address value, the second clock signal having essentially the same frequency as the first clock signal but being phase shifted with respect to the first clock signal by about 180°/*N*; and

outputting read data on a different bus than write data.

16. The method of claim 15, wherein:

in a read operation,

the step of accessing the first of *N* memory cell arrays includes latching a read address on first-type edges of the first clock and latching write addresses on second-type edges of the first clock; and

the step of accessing the second memory cell array includes latching a read address on first-type edges of the second clock and

latching write addresses on second-type edges of the second clock.

17. The method of claim 15, further including:

in a burst mode,

the step of accessing the first of *N* memory cell arrays includes accessing each of *M* sections of the first memory cell array in synchronism with different first-type and second-type edges of the first clock; and

the step of accessing the second memory cell array includes accessing each of *M* sections of the second memory cell array in synchronism with different first-type and second-type edges of the second clock.

18. The method of claim 17, further including:

in a read operation, outputting *N* * *M* read data values within the duration of a first clock signal cycle in response to a single read address.

19. The method of claim 15, further including:

in a read operation, outputting read data from the first memory cell array in synchronism with an output clock having essentially the same frequency as the first clock signal, and outputting read data from the second memory cell array in synchronism with second output clock having essentially the same frequency as the first clock signal; wherein

the read data is output from the second memory cell array with

about a 180°/*N* phase shift with respect to the output clock.

20. The method of claim 15, wherein:

in a write operation, the step of accessing the first of *N* memory cell arrays includes latching write data on first-type edges and second-type edges of the first clock; and

the step of accessing the second memory cell array includes latching write data on first-type edges and second-type edges of the second first clock.